Bahria University,

Karachi Campus



LAB EXPERIMENT NO.

12

LIST OF TASKS

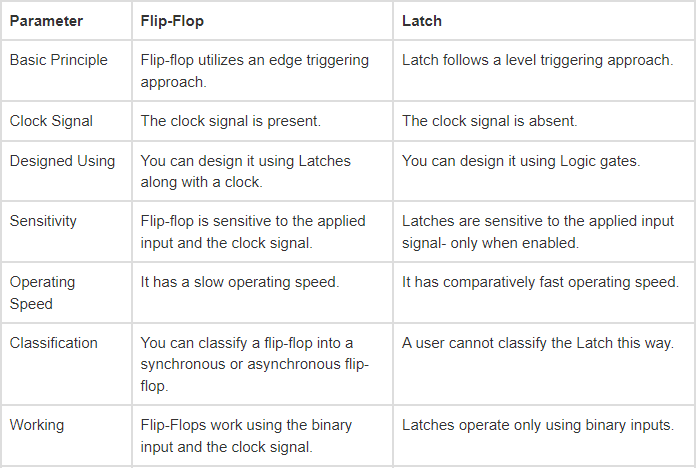
|  |  |
| --- | --- |
| **TASK NO** | **OBJECTIVE** |
| 01 | What is the difference between Flip-Flop and latch? |
| 02 | What is the difference between synchronous and asynchronous inputs? |
| 03 | What are the applications of different Flip-Flops? |
| 04 | What is the difference of Edge triggering over level triggering? |
| 05 | Design a circuit on MultiSim using D Flip Flop |
| 06 | Design a circuit on MultiSim using SR Flip Flop |
| 07 | Design a circuit on MultiSim using JK Flip Flop |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |

Submitted On:

(Date: DD/MM/YY)

**Task No. 1: What is the difference between Flip-Flop and latch?**

# Solution:



**Task No. 2: What is the difference between synchronous and asynchronous inputs?**

# Solution:

|  |  |
| --- | --- |
| **Asynchronous sequential circuit.** | **Synchronous sequential circuit.** |
| If some or all the outputs of a sequential circuit do not change (affect) with respect to active transition of clock signal, then that sequential circuit is called as **Asynchronous sequential circuit**. | If all the outputs of a sequential circuit change (affect) with respect to active transition of clock signal, then that sequential circuit is called as **Synchronous sequential circuit**. |

**Task No. 3: What are the applications of different Flip-Flops?**

# Solution:

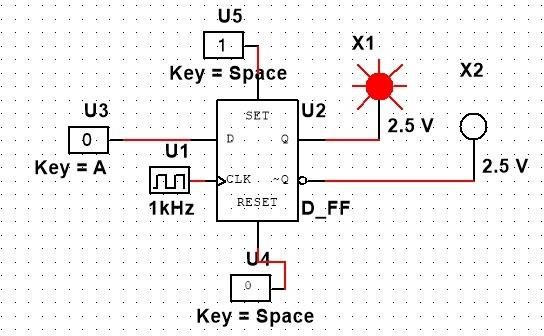
Application of the flip flop circuit mainly involves in bounce elimination switch, data storage, data transfer, latch, registers, counters, frequency division, memory, etc.

**Task No. 4: What is the difference of Edge triggering over level triggering?**

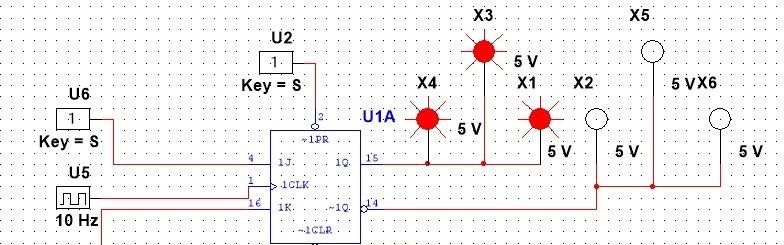
# Solution:

|  |  |
| --- | --- |
| **Edge triggering** | **level triggering** |
| If the sequential circuit is operated with the clock signal that is transitioning from Logic Low to Logic High, then that type of triggering is known as **Positive edge triggering**. It is also called as ***rising edge triggering***.    If the sequential circuit is operated with the clock signal that is transitioning from Logic High to Logic Low, then that type of triggering is known as **Negative edge triggering.** It is also called as ***falling edge triggering***. | If the sequential circuit is operated with the clock signal when it is in **Logic High**, then that type of triggering is known as **Positive level triggering**. It is highlighted in below figure.    If the sequential circuit is operated with the clock signal when it is in **Logic Low**, then that type of triggering is known as **Negative level triggering**. It is highlighted in the following figure. |

**Task #1:** Design a circuit on MultiSim using D Flip Flop?

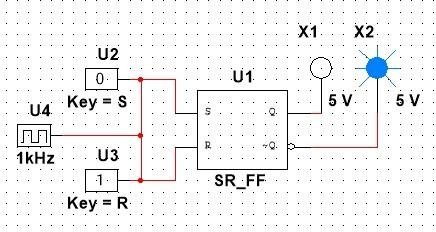


TruthTable



|  |  |  |
| --- | --- | --- |
| **C** | **D** | **Q** |
| 0 | X | No Change |
| 1 | 0 | Q=0 ; Reset State |
| 0 | 1 | Q=1 ; Set State |

**Task #2:** Design a circuit on MultiSim using SR Flip Flop?



TruthTable

|  |  |  |  |
| --- | --- | --- | --- |
| **C** | **S** | **R** | **Q** |
| 0 | X | X | No Change |
| 1 | 0 | 0 | No Change |
| 1 | 0 | 1 | Q=0 ; Reset State |
| 1 | 1 | 0 | Q=1 ; Set State |
| 1 | 1 | 1 | Indeterminate |

**Task #3:** Design a circuit on MultiSim using JK Flip Flop?

TruthTable

|  |  |  |
| --- | --- | --- |
| **J** | **K** | **Q(t + 1)** |
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | Q(t)' |